Optimized Design of GaN Switching Capacitor Based Envelope Tracking Power Supply for Satellite Applications

Qian Jin, Vasić M., García O. Alou P., Oliver J.A., Cobos J.A.

I. INTRODUCTION

With the development of the modem telecommunication, it is imperative to accelerate the data transmitting rate [1]. The radio frequency signals in those efficient modulations are featured with increasing bandwidth and higher peak-to-average power ratio (PAPR). As a consequence, the linear power amplifier (PA) (class A, B or AB) suffers from low efficiency. The most promising solutions are the Envelope Elimination and Restoration (EER) [2] and Envelope Tracking (ET) [3-4] techniques, which can greatly improve the efficiency of PAs. In the case of satellite applications, the weight that has to be launched to the space is of the outmost importance, and the reduced power losses can be seen as a decrease of the system weight, due to less heatsinking. Due to this reason, these techniques are gaining on importance in this area as well. In both techniques, ET and EER, the key element is a dc-dc converter called envelope amplifier or envelope tracker. Its task is to provide a varying voltage proportional to the envelope of the transmitted signal.

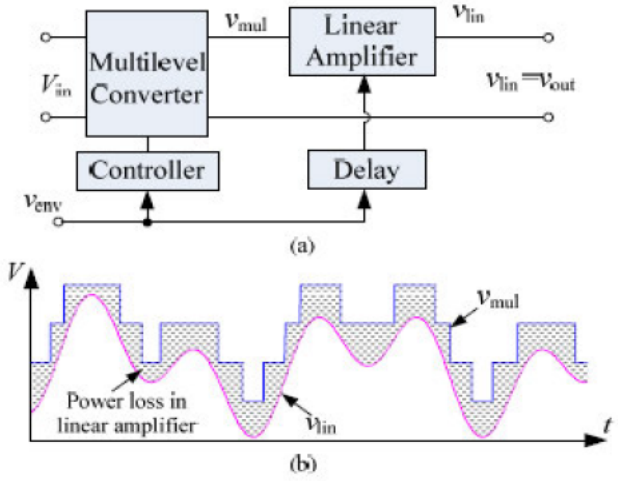

Fig. 1. Simplified schematic of the proposed envelope amplifier.

In the state of the art, there are various solutions for ET power supply, such as single switching-mode conveter [5], switching-mode converters in parallel [6-7], linear assisted switching-mode converter [8-9]. Due to the limited switching frequency, those solutions face the bottleneck to exceed bandwidth of several tens of kHz. Usually, to achieve 1 MHz tracking bandwidth, more than 5 MHz switching frequency is required [10]. Multilevel structure is a good candidate to increase equivalent switching frequency for a higher bandwidth. One of the solutions adopting a multilevel converter in series with a high slew rate linear amplifier [11] is shown in Fig. 1. Based on this idea, great effort is dedicated to explore a more practical multilevel converter in this paper, which helps reducing power loss and system weight.

A dc-dc converter based on switching capacitor is a good solution for high efficiency, as well as low weight and low occupied space. In [12] a switching capacitor based voltage divider is implemented with eight transistors, however, the three output voltage levels are dependent on each other. In this

paper, a novel switching capacitor based voltage divider is proposed to provide four alterable voltage levels with only four transistors, which offers more flexibility to optimize the design. GaN transistors have been selected as the switching device due to their resistance to single event upsets and, additionally, possibility to operate at high switching frequencies, which should decrease the weight and size of the envelope tracker. Two prototypes have been made, one with Si transistors and the other with GaN transistors, in order to compare the influence of these two technologies. The experiments were performed by tracking RF signals with bandwidth of 5MHz, while the maximum power was 40W.

II. PROPOSED SOLUTION

A. *Structure of the proposed multilevel converter*

The proposed multilevel converter consists of a switching capacitor based voltage divider and an analog multiplexer. A simplified schematic is presented in Fig. 2. The voltage divider can provide four voltage levels, and two of these are fixed as Vin (V_4) and Vin/2 (V_2). In order to maintain the middle voltage V_2 to be half of the input voltage, a flying capacitor is placed between two switching nodes A and B. In these nodes the voltage has a PWM shape and it changes between 0 and Vin/2 (node B) or between Vin/2 and Vin (node A). If a LC low pass filter is placed in these nodes an average voltage proportional to the duty cycle, D, can be obtained, just like in the case of a buck converter. Normally, in the case of the converters based on switching capacitors, the duty cycle is 50% [12]. But, in this solution this can be changed as it will be explained later. Thus, the four output voltage levels can be derived as D *Vin/2, Vin/2, (1+D) *Vin/2 and Vin. Obviously, those four voltage levels can be optimized for a higher overall efficiency with different duty cycle, which is a significant improvement comparing with the proposed solution in [12], where all the voltage levels are unalterable, proportional to the input voltage and obtained by combining two voltage dividers which increases the complexity of the system.

In the multiplexer, SW_i (i = 2, 3, 4) are the switches that turn on and off the corresponding voltage levels. The block diodes D_2 to D_4 are in series with SW_2 to SW_4, respectively, to avoid short circuiting of different voltage levels through the body diode of multiplexer transistors. As seen in Fig. 1(b), the power loss in the linear amplifier is proportional to the voltage difference between the output voltage of the multilevel converter and linear amplifier. It can be minimized if the voltage provided by the multilevel converter is close enough to the output voltage of the linear amplifier [13]. To realize this, the multiplexer is controlled to turn on and off these voltage levels depending on the characteristics of the envelope signals. Thus, it can supply the linear amplifier with voltage levels that are as close as possible to the output voltage of the linear amplifier. Since the multiplexer operates each switch only when the signal envelope crosses certain threshold level, its switching frequency is much lower than that in the traditional PWM multilevel converter. In this way, the proposed solution has a potential to achieve a higher tracking bandwidth applying relatively low switching frequency.

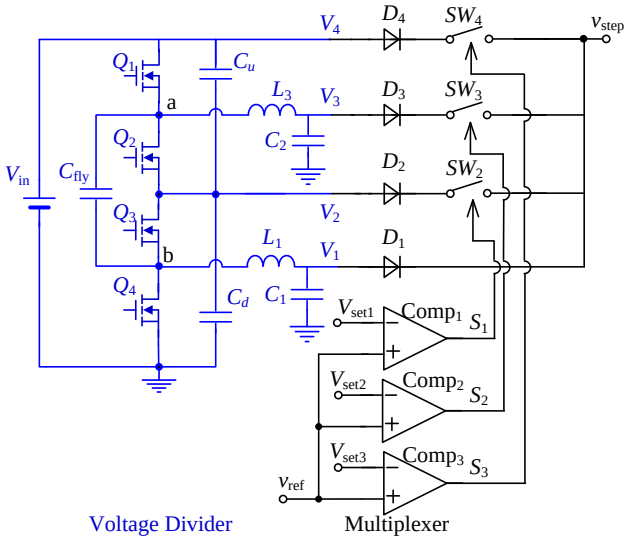

Fig. 2. Multilevel converter realized with switching capacitor based voltage divider and analog multiplexer.

In the proposed solutions, neither the voltage divider nor the analog multiplexer need precise control of its output voltage, because the linear amplifier that is put in series will perform the precise regulation, which means convenient open loop control can be adopted.

B. *Power loss model*

A detailed power loss model of the proposed structure is implemented to optimize all the design parameters for the highest efficiency. By combining the power loss model with the probability function of the transmitted signal ρ, the overall efficiency can be modelled precisely.

The power losses of the switching capacitor based voltage divider consist of three parts:

1. the switching losses in the employed transistors;
2. the power losses in the LC filter;
3. power losses in the switching capacitors.

The first two power loss mechanisms can be easily described as in the case of a fast-switching buck converter [15], and only the third mechanism will be analyzed in details in this paper.

The equivalent circuit of the voltage divider is illustrated in Fig. 3 (a), where I_1, I_2, I_3 are the average currents of correspond voltage levels. When Q_1 and Q_3 turn on, C_{fly} is connected in parallel with C_u, otherwise, C_{fly} is connected with C_d, as shown in Fig.3 (b) and Fig.3 (c), respectively. Therefore, when Q_1 and Q_3 are on, the currents in C_u, C_d and C_{fly} can be expressed as :

$$I_{cu\_on} = (I_1 + I_2) \cdot C_u / (C_{fly} + C_u + C_d) \quad (1)$$

$$I_{cd\_on} = (I_1 + I_2) \cdot C_d / (C_{fly} + C_u + C_d) \quad (2)$$

$$I_{cfly\_on} = (I_1 + I_2) \cdot C_{fly} / (C_{fly} + C_u + C_d) \quad (3)$$

And when Q_1 and Q_3 are off, the currents in C_u, C_d and C_{fly} can be expressed as :

$$I_{cu\_off} = (I_2 + I_3) \cdot C_u / (C_{fly} + C_u + C_d) \quad (4)$$

$$I_{cd\_off} = (I_2 + I_3) \cdot C_d / (C_{fly} + C_u + C_d) \quad (5)$$

$$I_{cfly\_off} = (I_2 + I_3) \cdot C_{fly} / (C_{fly} + C_u + C_d) \quad (6)$$

Therefore, the conduction loss in the switching capacitors can be derived as

$$P_{c\_con} = [D \cdot I_{c\_on}^2 + (1-D) \cdot I_{c\_off}^2] \cdot R_{esr} \quad (7)$$

For the transient when two capacitors or voltage source and one capacitor are connected together, the charge balance always exists. Here, we take the turn-on transient for example. And the power losses due to turn-off transient can be obtained accordingly.

Before the switching transient, C_{fly} is connected in parallel with C_d, and it is switched to C_u when Q_1 and Q_3 turn on. Therefore, the charge through C_{fly} and voltage source can be expressed as:

$$Q_{cfly} = Q_{cu} + Q_{cd} \quad (8)$$

$$Q_{vin} = Q_{cd} \quad (9)$$

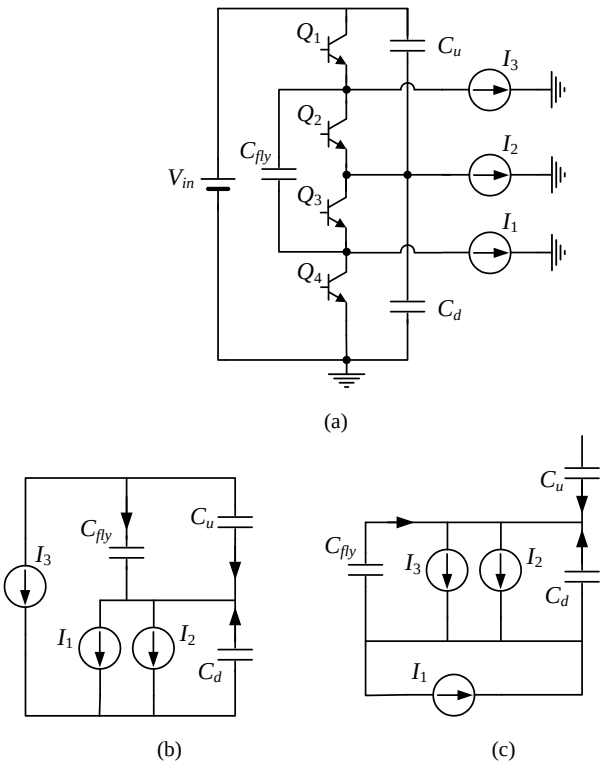

Fig.3 Equivalent circuits of the voltage divider.

As mentioned in [14], the inherent energy loss due to the voltage difference can be expressed as:

$$\Delta E_{tra} = \frac{C_{fly} \cdot (v_{cfly0+}^2 - v_{cfly0-}^2)}{2} + \frac{C_u \cdot (v_{cu0+}^2 - v_{cu0-}^2)}{2} + \frac{C_d \cdot (v_{cd0+}^2 - v_{cd0-}^2)}{2} + V_{in} \cdot Q_{vin} \quad (10)$$

Where the subscripts 0+ and 0− indicate the instants right before and after the switching transient, respectively.

As for the power losses in multiplexer and linear amplifier, the detail calculation can be found in [16]. Once the power losses of the complete converter have been modeled, the optimization algorithm can be started. Fig. 4 illustrates the theoretical efficiency of the proposed envelope amplifier for a 64QAM signals. As seen, the overall efficiency decreases slightly when the switching frequency in voltage divider increases. Therefore, the switching frequency in the voltage divider can be increased for a smaller volume. Besides, since most of the power are consumed in the linear amplifier, the voltage levels that are provided to the linear amplifier are critical for the overall efficiency. In the case of a 64QAM signal, the highest efficiency always presents at duty cycle of 0.4, regardless of the switching frequency in voltage divider.

The relationships between the efficiency and the capacitance of C_u and C_{fly} are illustrated in Fig 5. As seen, large capacitance of C_u benefits the overall efficiency, but, it goes against the requirement of the small volume and weight in satellite application. Moreover, according to (5), the capacitance of C_{fly} affects the amplitude of conduction current through the transistors. The smaller capacitance of C_{fly} can decrease the conduction current, which reduces the switching losses, however, increases the conduction loss in C_u and C_d. Thus, the selection of C_{fly} should be a result of the optimization of the overall losses.

Fig.6 illustrates the efficiency depending on the ripple currents of L_1 and L_3, where Δi_{L1} and Δi_{L3} refer to the ratios of the ripple current and average current. As seen, the highest efficiency presents when ripple currents equal to two times of the average current. It is the condition for high side transistors to achieve zero current/voltage switching.

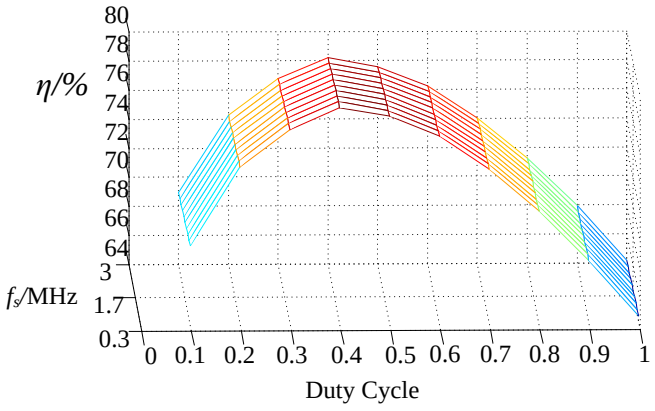

Fig. 4. Efficiency of the envelope amplifier depending on the duty cycle and switching frequency in voltage divider, in the case of a 5MHz 64QAM signal.

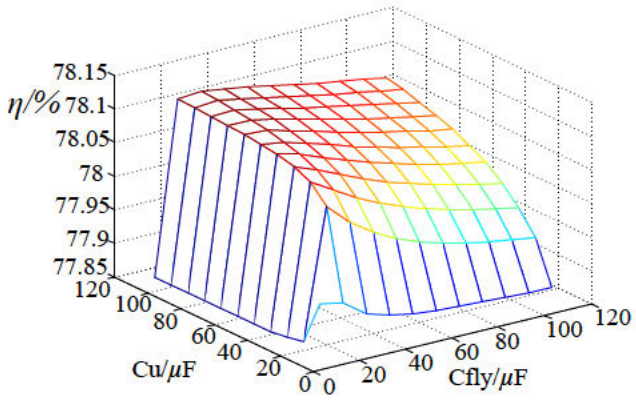

Fig. 5. Efficiency of the envelope amplifier depending on the capacitance of C_u and C_{fly}, in the case of a 5MHz 64QAM signal.

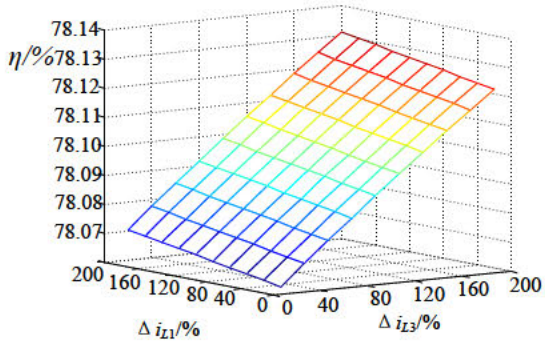

Fig. 6. Efficiency of the envelope amplifier depending on the ripple currents of L1 and L3, in the case of a 5MHz 64QAM signal.

III. Designed System

In order to verify the proposed switching capacitor based ET power supply, two prototypes have been fabricated (GaN and Si based) shown in Fig. 7. The specifications are as follows:

- Output voltage: 0 ~ 24 V;
- Peak output power : 40 W;
- Maximum tracking frequency: 5 MHz;
- Load resistance: 15 Ω.

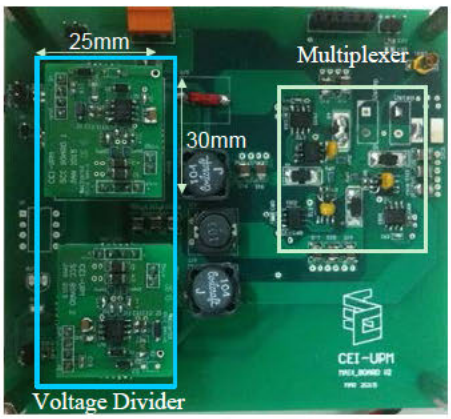

Fig. 7. Photograph of the implemented multilevel converter

As it is aforementioned, the voltage divider works with open loop control, and, in order to guarantee stable voltages at their outputs, at each output there are two ceramic capacitors in parallel (each one of 22 μF). Also, as mentioned above, the selection of C_{fly} should be a trade off between the power loss and system volume and in this design three 10 μF ceramic capacitors are placed in parallel.

To make a fair comparison, all the parameters except the transistors are kept the same in two prototypes. The detail implementations are listed in Table 1.

The triggering logic is implemented in a FPGA that is used as a source of the digital signal reference. The digitalized signal reference is sent to a D/A converter and from there to the linear amplifier. The same reference signal is sent to the triggering logic and to the linear amplifier. To synchronize these two voltages, a digital delay filter is implemented in the FPGA as well, in order to compensate the delays in the system and synchronize the multilevel output voltage with linear amplifier's reference.

IV. Experimental Results

Fig. 8 and Fig. 9 illustrate the comparison between the measured and estimated efficiency of the first stage (voltage divider stage with buck converters) over different switching frequencies and duty cycles. The solid lines indicate the efficiency curve of calculated results and the dotted lines indicate the measured results. As seen, there is a good agreement between the theoretical efficiency and the measurement, which proves the effectiveness of the power loss model. It also can be seen that the efficiency is inversely related to the switching frequency, however, is almost independent of duty cycle. Therefore, for a higher efficiency the switching frequency of the voltage divider can be lowered. On the other hand, the selection of the duty cycle mainly depends on the efficiency of the linear amplifier. It is important to note that there is little difference between GaN and Silicon devices when switching frequency is lower than 500 kHz. Thus, the GaN devices are more suitable for designs with switching frequencies in MHz range in which the converter should work in order to minimize the overall size.

Table I: Parameters of the Prototype

	Si prototype	Gan prototype
Transistors in Voltage divider	EPC2014	FDMS7620S
Transistors in analog multiplexer	EPC2014	Si4840DBY
Schottky diodes	VSSAF3L45-M3	
Drivers in voltage divider	LM2726	
Drivers in multiplexer	EL7158	
Isolator	ISO721	

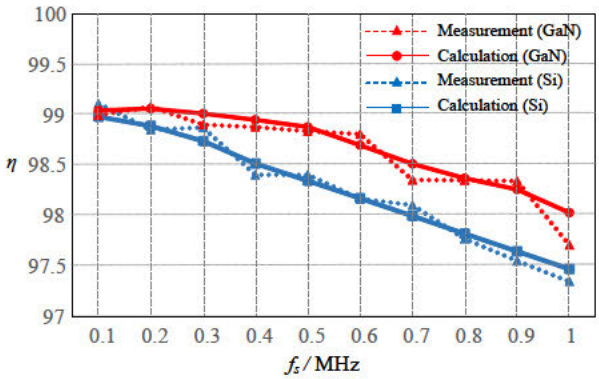

Fig. 8. Efficiency comparison over different switching frequencies when the duty cycle is selected as 0.5

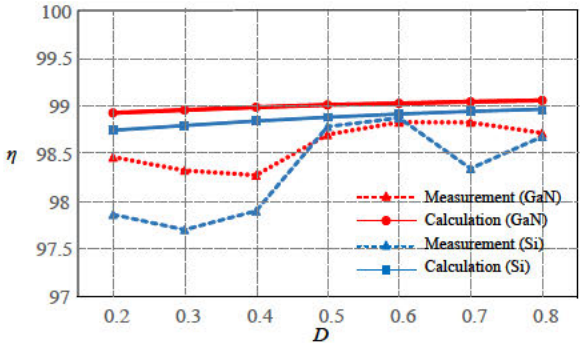

Fig. 9. Efficiency comparison over different duty cycles when the switching frequency is selected as 150 kHz.

To verify the effectiveness of the proposed solution, the multilevel converter has been tested with different sine-wave signals. Fig. 10 and Fig. 11 show the multilevel output voltage in the case when a reference is a sine-wave of 600 kHz and 3.6 MHz, respectively. The duty cycle for voltage divider is selected as 0.4 in this case. As seen, due to the stray inductors and parasitic capacitors, there is always an additional voltage spike when voltage is switched from one to another level. To reduce those parasitic parameters, special consideration has been paid to the PCB layout:

1. All switches in multiplexer are kept close to each other;

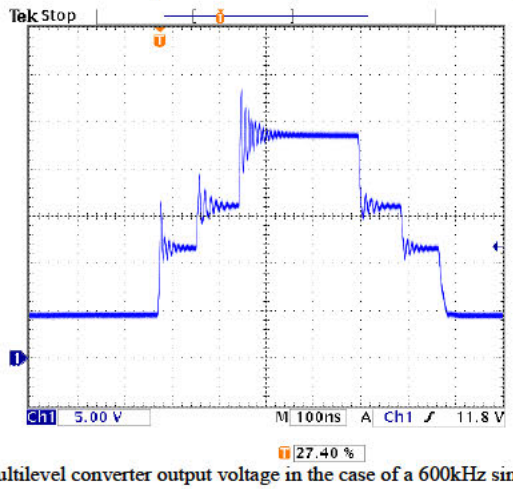

Fig. 10. Multilevel converter output voltage in the case of a 600kHz sine wave

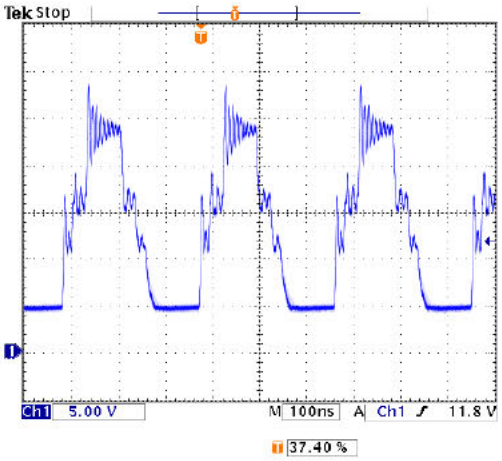

Fig. 11. Multilevel converter output voltage in the case of a 3.6 MHz sine wave.

2. The coper fill of step voltage is reduced for smaller inter-layer distributed capacitors.

Unfortunately, the oscillations are always present and may compromise the functionality of the envelope tracker.

Fig. 12 depicts the efficiency of the multilevel converter over different tracking frequencies in the case of a sine wave envelope. The efficiency is measured using a resistor as the load of multilevel converter. Since the switching loss for the multiplexer is related to the tracking frequency, the overall efficiency decreases along with the rising tracking frequency. However, the lowest efficiency, occurs at 3.6 MHz tracking frequency, is still higher than 90%. Furthermore, the implemented prototype was tested with a 5 MHz bandwidth 64QAM signal, as shown in Fig.13. The measured efficiency of the multilevel converter was 96.15% while the efficiency of the overall system was 75%, which shows a great improvement comparing with the multilevel converter based on independent voltage cells [11]. Fig.14 illustrates the measured overall efficiency over different duty cycles， when switching frequency in voltage divider is 150 kHz. As seen, the highest efficiency is obtained when the duty cycle of the first stage is 0.4, which shows a good agreement with the expected maximum obtained by theoretical analysis. The average output power was, approximately, 8W.

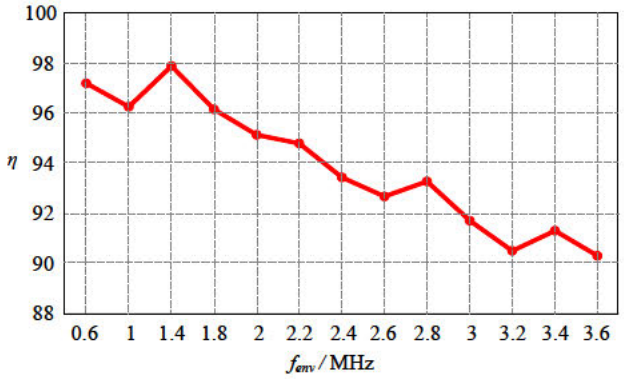

Fig. 12. Efficiency of multilevel converter for different frequencies of the tracked sine waves.

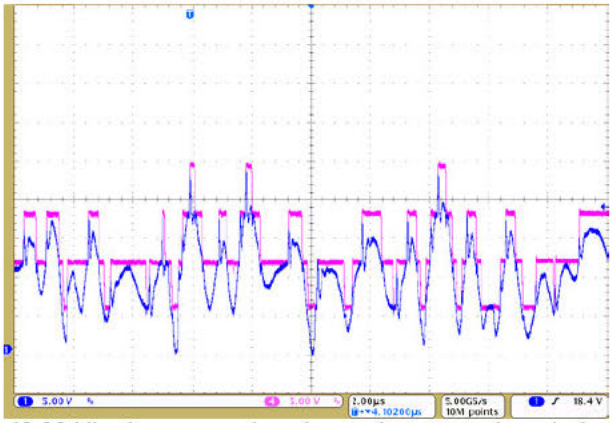

Fig. 13. Multilevel converter and envelope tracker output voltages in the case of a 5 MHz 64QAM signal.

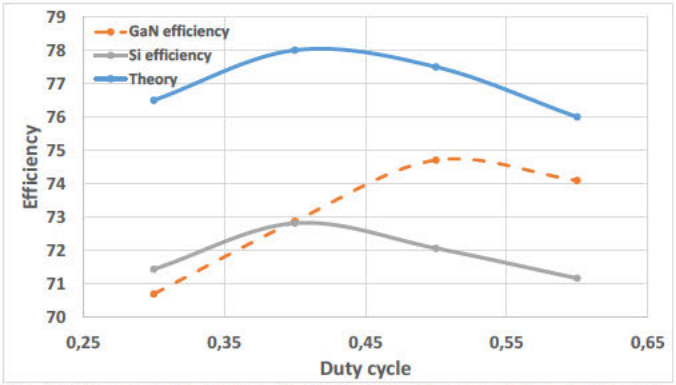

Fig. 14. Measured efficiencies of envelope amplifier over different duty cycles in the case of a 5 MHz 64QAM signal.

V. CONCLUSIONS

In this paper, a solution for envelope tracking power supply in ET technique is presented. It consists of a multilevel converter in series with a linear amplifier. A switching capacitor based voltage divider in combination with two LC filters is proposed to provide four individual voltage levels. The output voltage levels can be conveniently modulated by alterable duty cycle to maximize the efficiency of the linear amplifier, according to the tracking signals' characteristics. All the transistors are implemented with GaN device to further enhance the overall efficiency. Two prototypes (GaN and Si based) are built to verify the effectiveness of the proposed multilevel converter, which is capable of following a 5 MHz RF signal with maximum output power of 40W. The measured efficiency of the multilevel converter was 96.15% and the overall efficiency was around 75%. The experimental results show that for the switching frequencies in MHz range GaN transistors offer better efficiency than Si devices. This is of crucial importance due to the fact that the size and weight of the proposed converter is dramatically reduced using switching frequencies in this range

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References

[1] Z. Wang, "Demystifying envelope tracking: use for high-efficiency power amplifiers for 4G and beyond," IEEE Microwave Magazine, vol. 16, no. 3, pp. 106-129, Apr. 2015.

[2] C. Chen, Y. Lin, T. Horng, K. Peng, C. Li, "Kahn envelope elimination and restoration technique using injection-locked oscillators," in IEEE MTT-S, 20012, pp. 1-3.

[3] O. Lazaro and G. A. Rincón-Mora, "Comparative efficiency analysis of dynamically supplied power amplifiers (PA)," in IEEE ICECS, 2010, pp. 607-610.

[4] F. Wang, D. F. Kimball, J. D. Popp, A. H. Yang, D. Y. Lie, P. M. Asbeck, and L. E. Larson, "An improved power-added efficiency 19-dBm hybrid envelope elimination and restoration power amplifier for 802.11g WLAN applications," IEEE Trans. Microw Theory Tech., vol. 54, no. 12, pp. 4086-4099, Dec. 2006.

[5] D. Diaz, O. Garcia, J. A. Oliver, P. Alou, Z. Pavlovic and J. A. Cobos, "Ripple cancellation technique applied to a synchronous buck converter to achieve a very high bandwidth and very high efficiency envelope amplifier,". IEEE Trans. Power Electron., vol. 29, no. 6, pp. 2892-2902, Jan. 2013.

[6] A. Kanbe, M. Kaneta, F. Yui, H. Kobayashi, N. Takai, T. Shimura, H. Hirata, and K. Yamagishi, "New architecture for envelope-tracking power amplifier for base station," in IEEE APCCAS, 2008, pp. 296-299.

[7] P. Y. Wu and P. K. T. Mok, "A two-phase switching hybrid supply modulator for RF power amplifiers with 9% efficiency improvement," IEEE J. Solid-State Circuits, vol. 45, no. 12, pp. 2543-2556, Dec. 2010.

[8] P. F. Miaja, M. Rodriguez, A. Rodriguez, and J. Sebastian, "A linear assisted DC/DC converter for envelope tracking and envelope elimination and restoration applications," IEEE Trans. Power Electron., vol. 27, no. 7, pp. 3302-3309, Jul. 2012.

[9] H. Xi, Q. Jin, X. Ruan, and X. Xiong, "Full feed-forward of the output voltage to improve efficiency for envelope-tracking power supply using switch-linear hybrid configuration," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 451-456, Jan. 2013.

[10] L. Marco, E. Alarcon and D. Maksimovic, "Effects of switching power converter nonidealities in Envelope Elimination and Restoration technique", in IEEE International Symposium on Circuits and Systems, 2006, pp. 21-24.

[11] M.Vasić, O.Garcia, J.A.Oliver, P.Alou, D.Diaz and J.A.Cobos, "Multilevel power supply for high efficiency RF amplifier", in 24th Annual IEEE Applied Power Electronics Conference, 2009, pp. 25-30.

[12] M. Vasic, O. Garcia, J. A. Oliver, P. Alou, D. Diaz and J. A. Cobos, "Switching capacities based envelope amplifier for high efficiency RF amplifiers," in IEEE APEC, 2010, pp. 723-728.

[13] J. Hoversten and Z. Popovic. "Envelope tracking transmitter system analysis method," in IEEE RWS 2010, 2010, pp. 180-183.

[14] S. Ben-Yaakov, "Switched capacitors converters," in Professional Education Seminar at the 24th Annual IEEE Applied Power Electronics Conference, 2009.

[15] M Paolucci,"Advanced design for fast switching power mosfets," in Professional Education Seminar at the 26th Annual IEEE Applied Power Electronics Conference, 2011.

[16] M. Vasic, O. Garcia, J. A. Oliver, P. Alou and J. A. Cobos, ")Serial or parallel linear-assisted switching converter as envelope amplifierptimization and comparison," in IEEE ECCE, 2011, pp. 2488-2494.